



Very-Large-Scale Integration - Curriculum

SI.No	Topic
1	Orientation
1.1	Introduction Overview of M. Stepures
1.2 1.3	Overview of VLSI course Evolution if VLSI
1.4	VLSI Design Flow
2	Introduction to Digital World
2.1	Introduction, Number System
2.2	Logic Design
2.3	Boolean Algebra
2.4	Combinational Circuits
2.5	More Combinational Circuits
2.6	Sequential Circuits
2.7	Switch Debounce
2.8	Timing Analysis
3	Introduction to Semiconductors
3.1	Semiconductors, BJT, FET
4	Introduction to FPGA
4.1	Introduction and Architecture
5	Introduction to Digital Design with Verilog HDL
5.1	Typical Design Flow
5.2	Hierarchy Modelling
	r nor ar or ry readining
5.3	Basic Concepts
5.3 5.4	
	Basic Concepts
5.4	Basic Concepts Modules and Ports
5.4 5.5	Basic Concepts Modules and Ports Gate-Level Modelling
5.4 5.5 5.6	Basic Concepts Modules and Ports Gate-Level Modelling Dataflow Modelling





Very-Large-Scale Integration - Curriculum

PROJECT		
1	Basic circuits written in Verilog HDL, simulated and implemented on the FPGA	
2	Digital Design	
3	Image Processing on FPGA	
4	UART communication to print a single character	
5	FSM Designs-Mealy & Moore Machines and Up Down Counter	